In the Specification

Please amend the last paragraph beginning on page 2, line 26, as follows:

--The present invention is based on the ~~realisation~~ realization that the processes of the computer could be implemented with higher performance if only the memory stored in the data cache is used. For example, in a system in which there are several processors, performance would be improved if one or more of those processors used only their respective internal data caches. This higher performance may result from either or both of faster memory access and reduced external memory requirements.--

Please amend the third paragraph on page 3, line 17, as follows:

-- The processor (s) can also be connected, [[e. g.]] e.g., via the dummy interface, to an external memory [[chip]] chip, which provides data to ~~initialise~~ initialize the data cache.--

Please amend the last paragraph on page 4, line 22, as follows:

-- In an ~~initialisation~~ initialization stage, the dummy interface 13 reads data (including program ~~code)~~ code), which is required to ~~initialise~~ initialize the CPU 3 from the memory 19 into part of the data cache 7.--

Please amend the first paragraph on page 5, line 1, as follows:

-- Subsequently, in operation, the processor 1 operates exactly as in present systems. However, the program code which it runs ([[i. e.]] i.e., the program code uploaded from the memory 19 during the ~~initialisation~~ initialization) is such that the amount of memory required by the processor 1 is provided by the data cache 7. The cache controller 5 operates in the

conventional manner, performing write operations to the data cache 7 and attempting to keep an (in fact non- existent) external memory 17 updated to mirror what is in the data cache 7 by transmitting write operations to the system bus 11. These write instructions are passed to the dummy interface [[13]] 13, which simply discards the data it receives.--

Please amend the second paragraph on page 5, line 12, as follows:

--The address decoder 15 operates in a way similar to that of the prior art decoder discussed above, but with the difference that it never directs read/write commands from the CPU to the external memory 9. Write commands from the CPU 3 are simply discarded by the dummy interface 13 and the decoder 15. In the case that the dummy interface receives a read command from the CPU 3 (as in some embodiments it may do during the initiation procedure), the dummy interface transmits an output which is not dependent on the data which has previously been transmitted to it, [[e.g.]] e.g., it may always output"0". This feature may be used during an ~~initialisation~~ initialization of the data cache 7 in which portions of the memory which are not copied from the external memory 19 may be ~~initialised~~ initialized to zero using values read from the dummy interface 13.--

Please amend the third paragraph beginning on page 5, line 26, as follows:

-- We now ~~analyse~~ analyze the situation from the perspective of the CPU 3. The operation of the CPU is identical to what it would be if the dummy interface were not just discarding data, but instead was a normal interface performing read/write operations to a memory 17, operating as shown in Fig. 3: that is, not storing ("N/C") any data written to it, and

always outputting the value"0"in any read operation. In fact, this memory 17 does not exist, but the CPU 3 has no way of "knowing" this.--

Please amend the first full paragraph on page 6, line 3, as follows:

--Since the program code is such that the only memory required is provided by the data cache 7, the processor 1 operates in exactly the same manner as it would in the system of Fig. 1 running the same code. However, the system of Fig. 3 has the advantage that less memory is required, since the external memory 19 of Fig. 3 is only required to store the ~~initialisation~~ initialization data and may be smaller than the memory 9 of Fig. 1.--

Please amend the second full paragraph on page 6, line 9, as follows:

--Turning to Fig. 5, the address map for the system is shown. In this case, the memory space of the CPU 3 is entirely defined by the data cache 7. A portion 14 of the data cache stores ~~data~~ data, which was read from the external memory 19 during ~~initialisation~~ initialization, and this section is not overwritten during the operation of the processor 1. A second portion 16 of the data cache 7 is the read/write area which the processor 1 uses to perform its calculations. A portion 18 of data cache 7 is"reserved", [[i. e.]] i.e., unused in the operations of the processor 1.--

Please amend the last paragraph beginning on page 6, line 17, as follows:

-- Note that the CPU 3 may be one of a plurality of processing units which are part of the data processing system, such as ~~the shown~~ is shown in Fig. 6 having a master processing unit 20 and a plurality of slave processing units 21. In this case, one or more of the CPU processing units (~~e. g.~~ e.g., the master processing unit 20 only) may be provided with an external memory [[23]]

23, which is kept updated to mirror that processing unit's internal data cache by a conventional method such as that described above in relation to Fig. 1. Other of the CPU processing units (~~e. g.~~ e.g., some or all of the slave processing units 21) may be as discussed above in relation to Fig. 3, ~~i. e.~~ i.e., not being able to store data ~~an external~~ in external memory but instead performing processing only using their internal data caches and transmitting their write instructions to dummy interfaces [[25]] 25, which discard them. The dummy interfaces ~~initialise~~ initialize the slave processing unit 21 using one or more memory chips [[29]] 29, which do not store data during the subsequent processing operation. In this way, the overall performance of the system is improved, since fewer read/write memories 23 are required. At the same time, the processing speed of the system is improved since many of the processors (~~e. g.~~ e.g., the slave processing units 21) never need to wait to obtain data from external memories.--